A High-Performance 2–18.5-GHz Distributed Amplifier—Theory and Experiment

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Abstract—**A high-performance 2–18.5-GHz monolithic GaAs MESFET distributed amplifier has been designed and fabricated. The distributed amplifier is analyzed theoretically using a normalized transmission matrix approach, and a closed-form gain equation is presented for the MMIC *m*-derived drain-line case. Theoretical predictions are compared to measured results and more complicated CAD models. The measured small-signal gain is typically 8.0±0.40 dB from 2–18.5 GHz at standard bias. Typical input return loss is greater than 12 dB, and the output return loss is greater than 15 dB. The saturated output power is in excess of 23 dBm over most of the band, and the noise figure is less than 7.5 dB.**

I. Introduction

THE DISTRIBUTED AMPLIFIER is based on the principles of the artificial transmission line. Zobel [1] first formalized the theory of these networks in 1924 using iterative impedance and propagation functions. The idea of absorbing the input and output capacitance of an active device into artificial transmission lines was first implemented in vacuum-tube amplifiers by Percival [2] and later by Ginzton *et al.* [3]. The MESFET distributed amplifier has received much attention because of its extreme broad-band behavior and relative ease of realization in monolithic form.

Experimental results have been published for GaAs MMIC distributed amplifiers using *m*-derived drain-line topology [4]–[6]. The *m*-derived artificial transmission-line section has an inductor in series with a capacitor as its shunt element. This is in contrast to the constant-*k* network, which has only a shunt capacitor. The new theory included in this paper leads to an expression for the gain of a monolithic distributed amplifier with an *m*-derived drain line taking into account the capacitance associated with transmission-line inductors. The theory applies to a general class of distributed amplifier with discrete sampling points on the input line which couple to discrete excitation points on the output line.

II. Theory

A formulation for the distributed amplifier network using a new normalized transmission matrix approach is presented in this paper. The normal approach taken is the ABCD matrix formalism [7]–[9], where total voltages and currents are related. It is difficult to get a feel for reflections, coupling, and other phenomena best associated with waves using an ABCD matrix approach. The normalized transmission matrix approach has the advantage of clearly displaying the traveling-wave nature of the distributed amplifier, even when the input and output lines are constructed of lumped elements. The formalism applies to distributed or lumped networks, but is most conveniently applied to discrete sampling and excitation as opposed to distributed sampling and excitation. This method can be generalized to analyze amplifiers constructed of coupled gate and drain lines, and nonuniform gate and drain lines. The unilateral *m*-derived case will be presented here.

By normalizing the signals on the gate and drain lines to the characteristic impedance of the lumped lines and then writing a transmission matrix for the four-port unit cell, it is possible to arrive at a simple expression for the signals on the gate and drain lines. It will be shown how this matrix equation can be reduced to an expression for S_{21} of a distributed amplifier with an *m*-derived drain line.

Consider the case of a voltage-dependent current source connected in parallel across a transmission line of characteristic impedance Z_{0b}. Normalizing the signals on the input and output lines using the scattering formalism, the wave quantities as shown in Fig. 1 are given by

$$b_n^{\pm} = \frac{V_{bn}}{\sqrt{Z_{0b}}} \pm i_{bn}\sqrt{Z_{0b}} \tag{1a}$$

$$a_n^{\pm} = \frac{V_{an}}{\sqrt{Z_{0a}}} \pm i_{an}\sqrt{Z_{0a}} \tag{1b}$$

where V_{an}, i_{an}, V_{bn}, and i_{bn} are the total voltages and currents at section n. The a denotes the input line (gate line) and b denotes the output line (drain line).

Since the current will split equally in both directions

$$b_n^- = b_{n+1}^+ = -i/2\sqrt{Z_{0b}} \tag{2a}$$

$$i = g_m V_{an} D(\omega) \tag{2b}$$

$$\omega = \text{radian frequency}$$

where $D(\omega)$ is the ratio of the controlling voltage of the voltage-controlled current source (VCCS) to the voltage at the gate transmission-line node. For an FET, under un-

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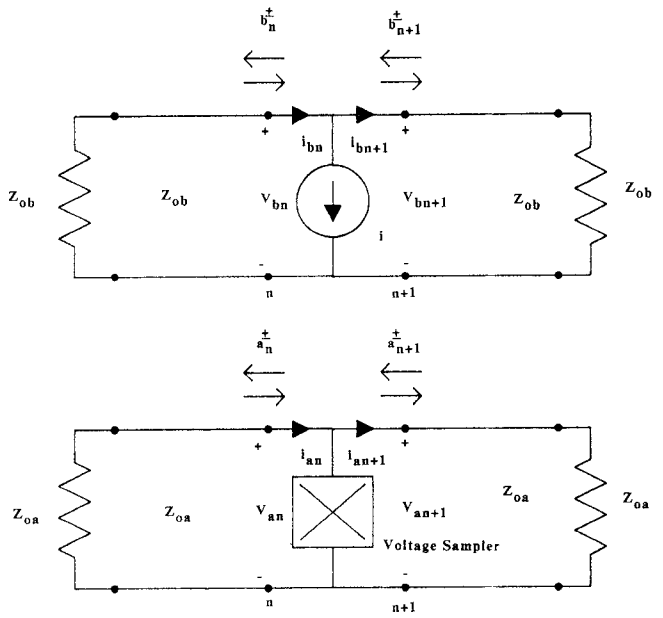

Fig. 1. Voltage-controlled current source coupling two transmission lines. The variables a_i and b_i represent incident and reflected waves on the input (gate) and output (drain) lines, respectively.

ilateral assumptions

$$D(\omega)=\frac{1}{1+j\omega/wg},\qquad \omega_g=\frac{1}{R_gC_g}. \tag{2c}$$

Substituting the expression for V_{an} into (1), we get

$$b_{n+1}^{+}=-\frac{1}{2}g_mD(\omega)\sqrt{Z_{0a}Z_{0b}}\,(a_n^{+}+a_n^{-}). \tag{3}$$

Since gate signals propagate along the gate line unaffected

$$a_n^{\pm}=a_{n+1}^{\pm}. \tag{4}$$

Incident signals on the drain line will superimpose on those signals generated at the controlled source, such that

$$b_{n+1}^{+}=H(a_n^{+}+a_n^{-})+b_n^{+} \tag{5a}$$

$$b_n^{-}=H(a_n^{+}+a_n^{-})+b_{n+1}^{-} \tag{5b}$$

where

$$H=-\frac{1}{2}g_mD(\omega)\sqrt{Z_{0a}Z_{0b}}\,. \tag{6}$$

Using the normalized transmission matrix formalism

$$w_{n+1}=\begin{bmatrix}1 & 0 & 0 & 0\\ H & 1 & H & 0\\ 0 & 0 & 1 & 0\\ -H & 0 & -H & 1\end{bmatrix}w_n \tag{7}$$

where

$$w_n=\begin{bmatrix}a_n^{+}\\ b_n^{+}\\ a_n^{-}\\ b_n^{-}\end{bmatrix}.$$

Define $[H]$ such that

$$w_{n+1'}=[H]w_n \tag{8}$$

where the prime denotes the signal vector at the right side of the controlled source before propagation through the transmission networks, as shown in Fig. 2.

The matrix $[H]$ describes the coupling of the gate and drain lines through the VCCS. We now transform the vector w_n through the section of transmission line which connects the controlled sources together. The signals on either side of the line section are related by attenuation and phase functions. The relationship is succinctly written as

$$w_{n+1}=[G]w_{n+1'} \tag{9a}$$

where

$$[G]=\operatorname{diag}\{\exp(-\theta_a),\exp(-\theta_b),\exp(\theta_a),\exp(\theta_b)\}. \tag{9b}$$

Note that the propagation constants θ_a and θ_b are complex. Now the subnetwork given by one VCCS and a section of line is described by the product of $[H]$ and $[G]$, so that

$$w_{n+1}=[T]w_n \tag{10a}$$

where

$$[T]\equiv[G][H]. \tag{10b}$$

Suppose we have a distributed amplifier with N voltage-controlled current sources. Suppose also that we have at the input side of this amplifier a set of incident and reflected waves on the input and output lines, which we will denote w_0. The wave amplitudes at the output of the amplifier are given by

$$w_N=[T]^Nw_0. \tag{11a}$$

This expression relates the input at the first VCCS to the output of the last whole section of input and output line. This asymmetry appears because we have characterized the lines in terms of the characteristic impedance that is presented to the VCCS. This is somewhat artificial because one cannot in practice get a whole VCCS with only a half-section shunt impedance, nor does one find whole sections on the output of distributed amplifiers. To arrive at the usual reference plane, one needs to rotate one half-section back on the input and output lines of the amplifier. The input vector is related to w_0 by

$$w_{\text{in}}=\left[G_{-1/2}\right]w_0 \tag{11b}$$

and the output vector is related to w_N by

$$w_{\text{out}}=\left[G_{-1/2}\right]w_N \tag{11c}$$

where

$$\left[G_{-1/2}\right]=\operatorname{diag}\{\exp(\theta_a/2),\exp(\theta_b/2),\exp(-\theta_a/2),\exp(-\theta_b/2)\}. \tag{11d}$$

Note that

$$\left[G_{-1/2}\right]^{-1}=\operatorname{diag}\{\exp(-\theta_a/2),\exp(-\theta_b/2),\cdot\exp(\theta_a/2),\exp(\theta_b/2)\}\equiv\left[G_{1/2}\right] \tag{11e}$$

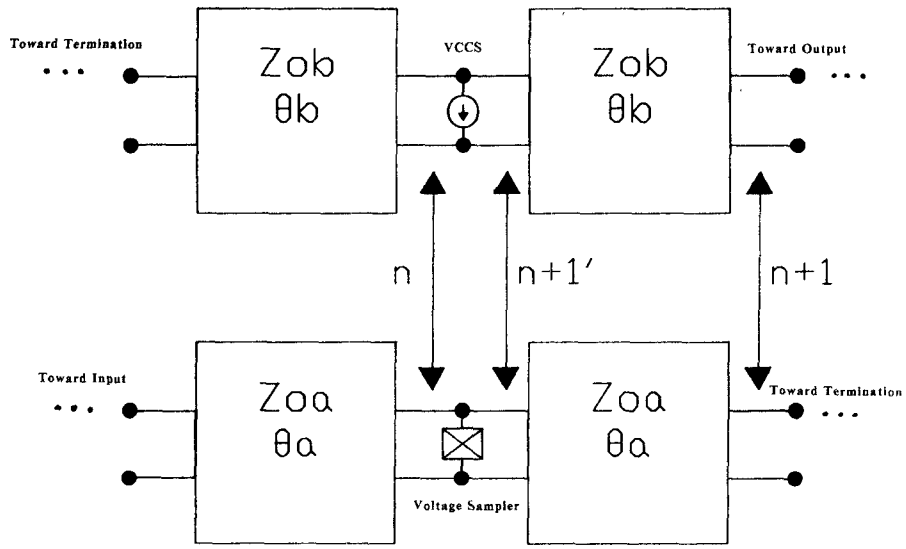

Fig. 2. Distributed amplifier schematic showing reference plane definitions used to distinguish between the VCCS along and the VCCS–transmission line section combination.

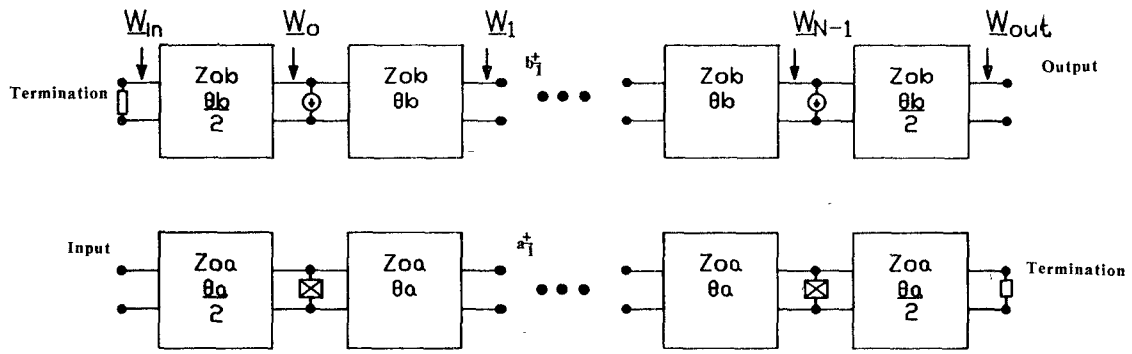

Fig. 3. Complete distributed amplifier showing reference planes used in the transmission matrix analysis.

so that the input and output variables are related by the following

$$\boldsymbol{w}_{\text{out}} = [\boldsymbol{G}_{-1/2}][\boldsymbol{T}]^N[\boldsymbol{G}_{1/2}]\,\boldsymbol{w}_{\text{in}}. \tag{11f}$$

The conventions used become apparent by referring to Fig. 3.

The next step in the analysis is to apply boundary conditions, which relate, for example, incident and reflected waves at the gate and drain line terminations. If we assume matched conditions at the terminations, we have that $a_N^- = 0$, $b_N^- = 0$ and $b_0^+ = 0$. We also have that $a_i = 0$, $i = 0,1,2,\cdots,N$; there is no reverse wave on the gate line. Since we are interested in the gain of the amplifier which will manifest itself strictly in forward-traveling drain signal, we can disregard the reverse propagating wave in pursuit of a gain expression for the uniform unilateral case. This is because the reverse-traveling wave propagates toward the drain termination, where it is absorbed, and none of it contributes to the gain of the uniform amplifier. In the following simplified analysis, we will use the reference planes implied in (11a), and the reference shift will be made in the last step. We have

$$\begin{bmatrix} b_{n+1}^+ \\ a_{n+1}^+ \end{bmatrix} = e^{-\theta_0}\begin{bmatrix} e^{\theta_d} & He^{\theta_d} \\ 0 & e^{-\theta_d} \end{bmatrix}\begin{bmatrix} b_n^+ \\ a_n^+ \end{bmatrix} \tag{12}$$

where

$$\theta_0 = \frac{\theta_a + \theta_b}{2} \qquad \theta_d = \frac{\theta_a - \theta_b}{2}$$

and θ_a and θ_b are the propagation functions of the gate and drain lines, respectively.

The matrix of (12) has the eigenvalues e^{θ_d} and $e^{-\theta_d}$ and associated eigenvectors

$$\begin{bmatrix} b_{e1} \\ a_{e1} \end{bmatrix} = a_0 \begin{bmatrix} \dfrac{-He^{\theta_d}}{2\sinh(\theta_d)} \\ 0 \end{bmatrix} \tag{13a}$$

$$\begin{bmatrix} b_{e2} \\ a_{e2} \end{bmatrix} = a_0 \begin{bmatrix} \dfrac{He^{\theta_d}}{2\sinh(\theta_d)} \\ 1 \end{bmatrix} \tag{13b}$$

where a_0 is an arbitrary constant. Note that the eigenvec-

tors satisfy the required boundary condition

$$b_0 = b_{e1} + b_{e2} = 0.$$

That is, there is no forward-traveling wave at the nonreflecting drain termination.

The signal at the output of N sections is given by

$$b_N^+ = \left(\lambda_{e_1}^N b_{e1} + \lambda_{e_2}^N b_{e2}\right) e^{-N\theta_0} \tag{14}$$

where λ_{e2} and λ_{e2} are eigenvalues associated with the eigenvectors. Rewriting (14), we get

$$\frac{b_N^+}{a_0} = \frac{H \sinh(N\theta_d)}{\sinh(\theta_d)} e^{-N\theta_0} e^{\theta_d}. \tag{15}$$

Equation (15) relates the incident gate signal at the first gate to the incident drain signal at the output of the last full section of the drain line. As discussed above, the reference plane for this expression is atypical; in a typical realization, the input line signal suffers one more half-section of phase shift than in (15) and the drain signal one less half-section phase shift than (15). Therefore, multiplying (15) by $e^{-\theta_d}$ yields an expression for S_{21} of the matched, unilateral distributed amplifier

$$S_{21} = \frac{b_N^+}{a_0} = \frac{H \sinh(N\theta_d)}{\sinh(\theta_d)} e^{-N\theta_0}. \tag{16}$$

Equation (16) is exact under the assumptions of 1) unilateral VCCS and 2) perfect match at input and output lines.

Up to now, the analysis has been quite general; there has been no need to specify the network that connects the devices, that is, the interconnecting section elements. The main characteristic of this description is that it applies to discrete sampling and excitation. In order to apply this theory to the case of the microwave distributed MESFET amplifier, we specify the input and output lines to be lumped and the input and output line generated from the network shown in Fig. 4. The tee-section is shown in Fig. 4 because it embeds a whole transistor; however, it is the pi-impedances that appear in the equation for H, so one must be able to generate pi-sections from the network. To do this, one need only bear in mind that the shunt element of the tee-section is equivalent to the parallel combination of two pi-section shunt elements. In order to apply the above formulation to the MMIC m-derived case, we need to find an equivalent circuit with the form of the network shown in Fig. 1.

The input (gate) line fits the form of the input line network of Fig. 1 without any modification; however, the drain line need to be manipulated. To do this, we compute a Thevinen and then a Norten equivalent, and the resulting drain circuit is simplified to that of Fig. 5, where

$$i' = \frac{i}{1 + \left(j\omega/\omega_{Ld} - 4\omega^2/\omega_{cd}^2\right)} \tag{17}$$

where

$$\omega_{cd} = \frac{2}{\sqrt{L_d C_d}}, \qquad \omega_{Ld} = \frac{1}{G_d L_d}.$$

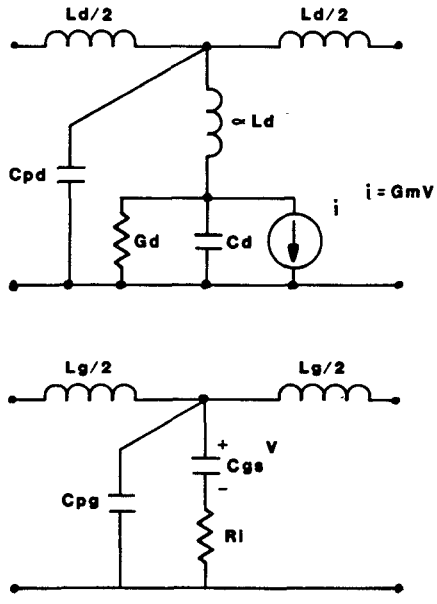

Fig. 4. M-derived drain line and constant-k gate line distributed amplifier section as realized in an MMIC. The parasitic C_{pd} distinguishes the MMIC realization of the m-derived drain line from a "pure" m-derived section.

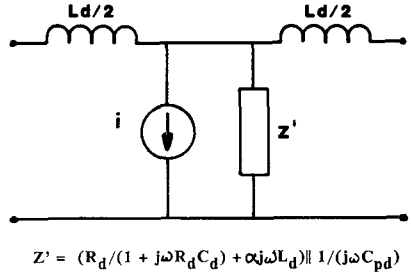

Fig. 5. Transformed m-derived drain line section. When transformed to this equivalent circuit, the network has the same form as in Fig. 1.

Substituting i' for i in (6) results in a new expression for H

$$H = \frac{-g_m\sqrt{Z_{\pi g} Z_{\pi d}}}{2\left(1 + j\omega/\omega_g\right)\left(1 + \alpha\left(j\omega/\omega_{Ld} - 4\omega^2/\omega_{cd}^2\right)\right)}. \tag{18}$$

Here, Z_{0a} and Z_{0b} have been replaced by $Z_{\pi g}$ and $Z_{\pi d}$, the pi-section image impedances [1] of the gate and drain lines in the equation for H.

In general, the normalized transadmittance is given by

$$H = \frac{-g_m}{2}\sqrt{Z_{\pi g} Z_{\pi d}}\, D_g(\omega)\, D_d(\omega) \tag{19}$$

where $D_g(\omega)$ is the gate voltage division term, and $D_d(\omega)$ is the drain current division term. The pi-section characteristic impedance of the drain line is computed using Z' from Fig. 5. The expressions include loss in both the gate and drain lines through the complex propagation constants and through the complex pi-section image impedances. The normalized transadmittance characterizes the forward coupling between the input and output lines and describes the gain mechanism per section.

For lumped-element, low-pass constant-k or low-pass m-derived networks, $|Z_{\pi g}|$ and $|Z_{\pi d}|$ are monotonically

increasing in the passband; therefore, $|H|$ is monotonically increasing, which combats the monotonically decreasing nature of $|e^{-N\theta_0}|$. This is in contrast to a continuously distributed traveling-wave transistor, in which the magnitude of the characteristic impedance will not increase as a function of frequency.

The $\sinh[N(\theta_d)/2]/\sinh[\theta_d/2]$ factor is related to the phase coherence between the two lines and its impact as the wave travels down N sections. The exponential factor is simply the average total phase and attenuation a signal must propagate through in getting from the input to the output. When considering more complicated structures, such as tapered or coupled lines, one may return to (10b) and its derivation to determine the matrix $[T]$ on a per-section basis.

As far as interpreting the m-derived case, which is the main thrust of this discussion, we see from (18) that the gain expression has a complex pole given by the series resonant frequency of the shunt branch and the drain resistance reducing the Q of the resonance. Notice that the parasitic capacitance C_{pd} does not modify the resonance, but reflects its presence in the drain propagation function and the drain-line characteristic impedance only. This capacitance, C_{pd}, is typically on the same order as, if not larger than, the output capacitance of the FET; so it influences the behavior of the drain line considerably. This will tend to make the line look somewhat like constant-k. This is an important result, since a perfect m-derived line has a phase function that follows the inverse tangent as a function of frequency, and the constant-k line follows an inverse sine. The gate line is obviously constant-k; therefore, significant phase deviation might be expected between the gate and drain lines in an m-derived drain line design, while in reality this effect is moderated by C_{pd}. A comparison of this theoretical expression with a more complicated model will be shown later.

Equations (16) and (19) together form a general expression for a distributed amplifier built with voltage-controlled current sources; this expression represents a convenient way to analyze otherwise arbitrary unilateral structures. Other types of controlled sources, such as current-controlled voltage sources or current-controlled current sources, can be used to implement distributed amplifiers as well as can be analyzed within this framework by rederiving (2) and (3) for that case.

III. Amplifier Design and Comparison with Theory

The theory discussed above was not complete at the time that the amplifier was designed, so a simple approximation and constant-k theory [10] were applied to arrive at a prototype circuit. The method taken was to choose the m-derived inductor length such that $C_{gs}/C_d - \omega^2 L_d C_{gs} = 1$ at the high end of the band. The lumped elements so obtained were converted to transmission lines. The model shown in Fig. 6. was fit to the measured FET S-parameters. All device parameters except L_s were scaled with gate width to yield a model considered valid from

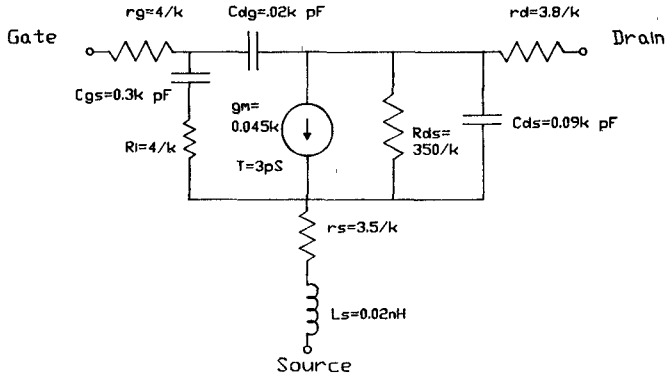

Fig. 6. MESFET scaling model (not including pad parasitics). The parameter k is the ratio of desired total gate periphery to 300 μm.

150 μm to 350 μm of total gate periphery. Above 350 μm, gate resistance and the distributed nature of the gate fingers degraded the model, while below 150 μm, interconnection parasitics reduced its accuracy. Using this scaling model, the prototype circuit was optimized to yield a flat gain of nearly 7 dB and low terminal VSWR. Finally, a square spiral inductor was added across the drain-line termination to allow insertion of bias. The one-and-three-quarters turn spiral was modeled using the work of Cahana [11] as the interconnection of a coupled microstrip line and a single microstrip line. Additional optimization using SuperCompact yielded the final prototype circuit.

The prototype was converted to a large (400×) layout. The layout showed clearly where coupling would be a problem ($k < 20$ dB) as well as pointing out the large number of microstrip bend, step, and tee junctions which would be unavoidable in the final circuit. The layout was carefully done to minimize the number of different discontinuities present, thus simplifying the overall circuit model and reducing the discontinuity modeling task significantly. Bends and tees in the narrow lines were found to have significant negative electrical length. Almost 1300 μm of line length had to be added to the prototype elements to compensate for the bends and tee junctions alone. The effect of coupling in the microstrip c-sections reduced the inductance of these lines, requiring more line length to be added. Situations that required a multiple coupled line model were avoided since none was available to use for design and optimization. The layout and complete circuit model were iterated several times until adequate circuit performance and consistent layout were obtained.

A sensitivity study was performed to assess the impact of process variables such as MESFET C_{gs}, C_{gd}, C_{ds}, R_i, R_{ds}, g_m, GaAs epitaxial sheet resistivity, and capacitor dielectric thickness. Sensitivity to model variation was also performed to determine sensitivity to errors in the bend and spiral inductor models. The sensitivity analysis revealed that FET g_m and C_{gs} were the most important process-dependent parameters and that the amplifier was relatively sensitive to the accuracy of the microstrip bend model.

Equation (16) was evaluated using lumped elements determined from y-parameters of the microstrip inductors

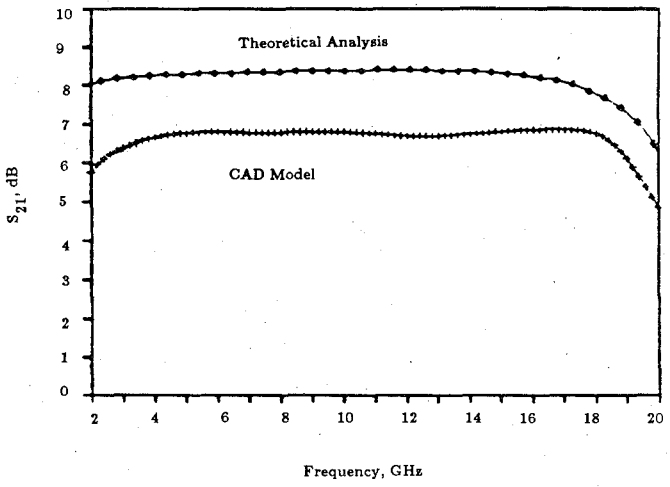

Fig. 7. Theoretical versus more complicated CAD model. The analytical expression shows more gain across the band, which is mostly due to the unilateral assumption of the theory. The low end rolloff in the SuperCompact model is related to the drain termination, whereas the slight tendency for rolloff in the theoretical expression is due to the behavior of the image impedance of the drain line.

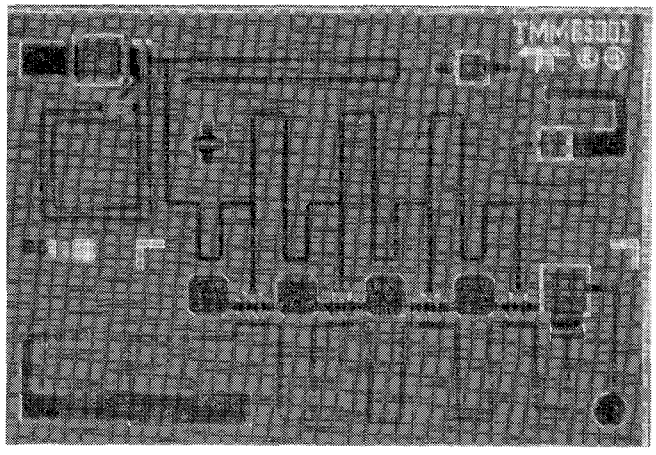

Fig. 8. TMM85001 Distributed Amplifier. The chip dimensions are 0.093 by 0.064 in.

as modeled on SuperCompact. Transistor R_g, C_{gs}, R_d, and C_{ds} were determined from the full-complexity overall circuit model discussed above. The CAD model and the analytical expression are compared in Fig. 7. The analytic expression tends to be optimistic by a maximum of 2.1 dB. It is our experience that the most significant omission in the theoretical expression is the effect of the gate-to-drain capacitance of the FET, and that this can account for most of the observed error. Frequency dependence of elements could account for some of the high-frequency discrepancy, such as the early rolloff. The midband gain discrepancy is due most likely to the effects of the feedback capacitance of the FET. Omissions such as microstrip loss are second-order, but can be taken into account in (16). The frequency dependence of the elements can be taken into account easily in theory, although the improvement in accuracy may not warrant the added complexity.

IV. Device Fabrication

The active layer on the GaAs wafers was prepared using ion implantation of 29Si directly into low chromium doped LEC substrates. The slices were annealed using the proximity technique, in conjunction with arsenic overpressure. The implant profile selected was a shallow, highly doped "low-noise" profile (one of several standard profiles available in the Texas Instruments GaAs Facility).

Device processing followed the normal production flow used in TI's Facility. Conventional contact photolithography, using the well-known chlorobenzene technique [12] to facilitate lift-off, was used in all masking steps except gate fabrication, which uses e-beam lithography.

Device isolation was achieved using mesa etching. This step also defines various GaAs resistors used on the MMIC. Ohmic contacts were fabricated using alloyed AuGeNiAu. Electron-beam lithography was next used to expose a 0.5-μm gate pattern. Wet chemical etching was used to "recess" the gate pattern down to a specified source–drain current, and the gates were metallized using TiPtAu. A TiAu "first metallization" was then fabricated, forming overlay metal (over ohmics), bottom capacitor plates, and transmission lines.

A 2000-Å layer of silicon nitride was applied using plasma-enhanced chemical vapor deposition. This material functions as the capacitor dielectric and also encapsulates gate areas of FET's. The top capacitor plates were formed using TiAu.

After patterning and etching away unwanted dielectric, the slices were plated using the conventional two-resist approach [13], which allows formation of air bridges. These air bridges were used to interconnect FET source pads and to connect top capacitor plates to adjacent metallization. Bonding pads, transmission lines, and top capacitor plates were also plated during this step.

At various times during the frontside processing, in-process electrical tests were performed using computer-controlled equipment. These measurements are made on test patterns contained in plug bars located at five positions on the slice. Such measurements ensure process integrity and also serve to identify out-of-specification slices so that these can be either reworked or scrapped before further economic investment is made. A number of in-process visual inspections were performed for similar reasons.

After frontside processing was complete, every chip on the slice was electrically probed by computer-controlled probers. This "autoprobe" dc data included saturation current, transconductance, pinchoff voltage, breakdown voltages of all FET's, and other data such as resistor values and capacitor integrity. The computer analyzed these data, providing statistical summaries and maps of good chip locations.

The slices were next mounted frontside down on a glass substrate for backside processing. After lapping the slice to 150 μm (0.006 in), the back was spun with resist and patterned for via-hole etching using an infrared aligner to align the via hole pattern to frontside alignment markers. The via holes were then etched using reactive ion etching. This technique (as opposed to wet chemical etching) yields

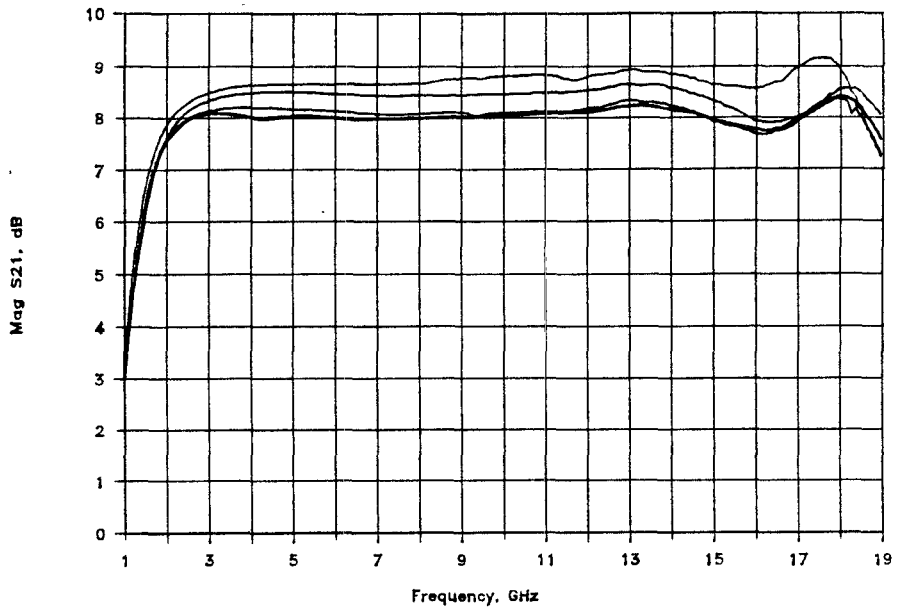

Fig. 9. Measured small-signal gain for four devices from a single wafer. The incident power was approximately −10 dB. The devices were biased at $V_{ds} = 5$V, $V_{gs} = -1$V; I_{ds} varied from 95 mA to 130 mA. The data shown are de-embedded from the microstrip launchers and alumina fixturing, up to but not including the bond wire inductances using the TSD technique [14].

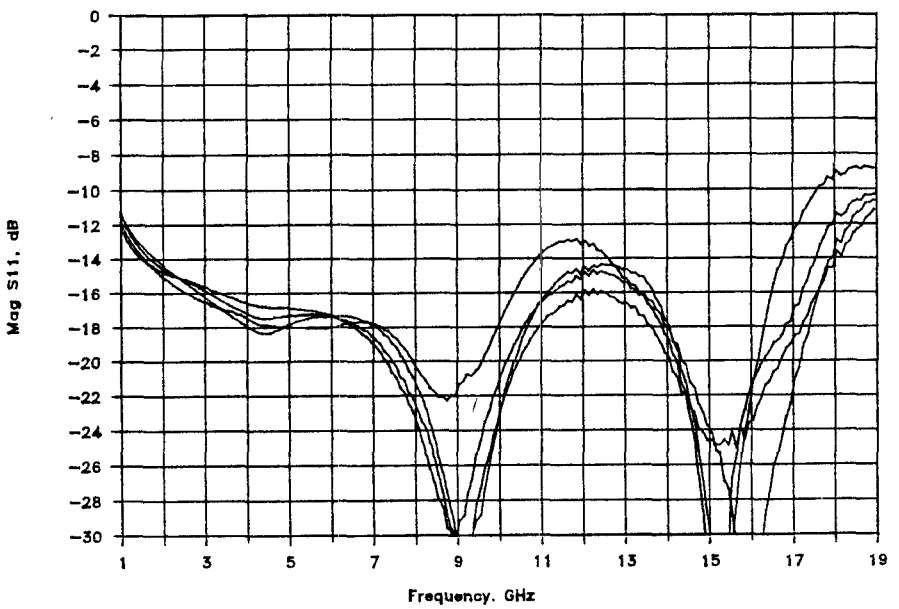

Fig. 10. Measured input return loss. Incident power is approximately −10 dBm. Data are de-embedded from launchers and alumina microstrip line. Data include effect of bond wires.

steep-walled via holes with minimal undercutting. The backside was then metallized and plated, forming a plated heat sink which also connects through the via holes to frontside metallization (the scribe streets between chips were not plated).

The slices were then transferred to a commercial, stretchable tape for sawing and expanding. The expanding operation retains the relative position of the chips. These can be removed from the tape based on the autoprobe data obtained earlier. These electrically good chips were then visually inspected before release.

V. Experimental Results

A picture of the amplifier is shown in Fig. 8. The device measures 0.093×0.064 in. Bias current is fed into the drain line through the large spiral inductor, shunting the resistive drain termination. The gate bias is applied through the gate-terminating resistor. Both points are bypassed to

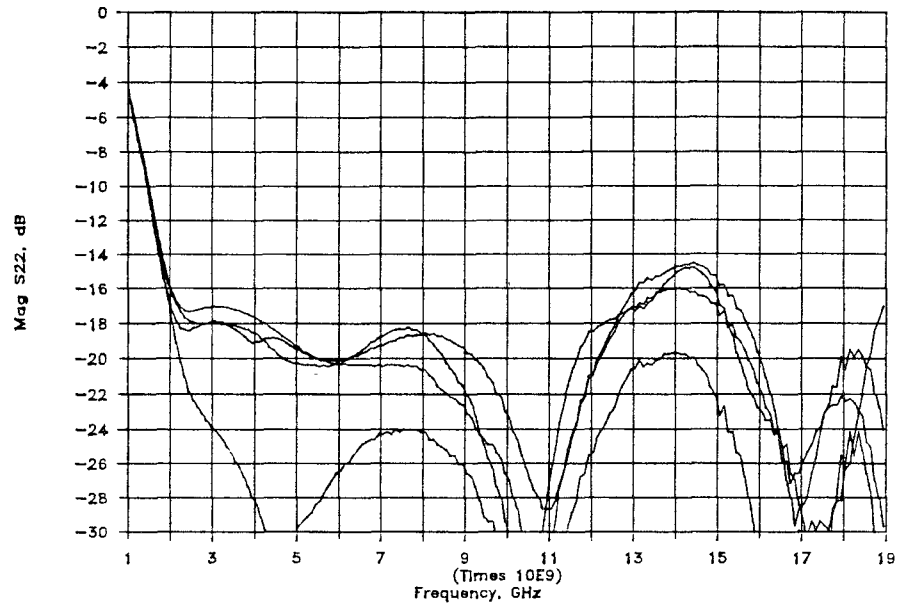

Fig. 11. Measured output return loss. Incident power is approximately −10 dBm Data are de-embedded from launchers and alumina microstrip line. Data include effect of bond wires.

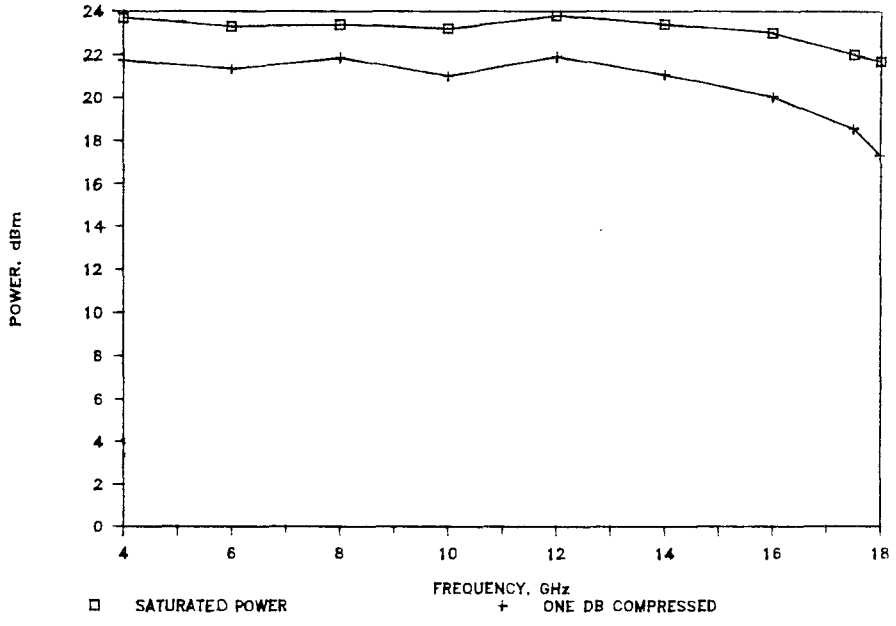

Fig. 12. Measured power saturation characteristic. Quiescent bias point was $V_{ds} = 6.5$V, $V_g = -1$V, $I_{ds} = 142$ mA.

ground through capacitors connected to via holes. The active elements are four 189×0.5-μm interdigital MESFET's.

Measured results of gain and return loss from several devices biased at −1 V on the gate of 5 V on the drain are shown in Figs. 9–11. The typical I_{dss} was 273 mA/mm and the pinchoff and breakdown voltages were approximately 2.5 V and 10 V, respectively. When the drain voltage is increased to 6.5 V, the saturated output power and 1-dB compressed power are as shown in Fig. 12. The gain at saturation was 2.3 dB at midband and the 1-dB compressed power gain is approximately 7 dB. The gain is relatively insensitive to changes in drain voltage for voltages above 5 V. A typical noise figure plot appears in Fig. 13.

While designed primarily as a small gain signal stage, the amplifier performs well in terms of output power and noise figure. When placed in an evanescent waveguide, a three-stage cascade provided gain of 22 dB $\pm$ 0.75 dB.

The experimental gain results are much higher than modeled because the transconductances of the FET's were 20 percent high.

A very high percentage of the devices that were tested to be dc functional were also RF functional.

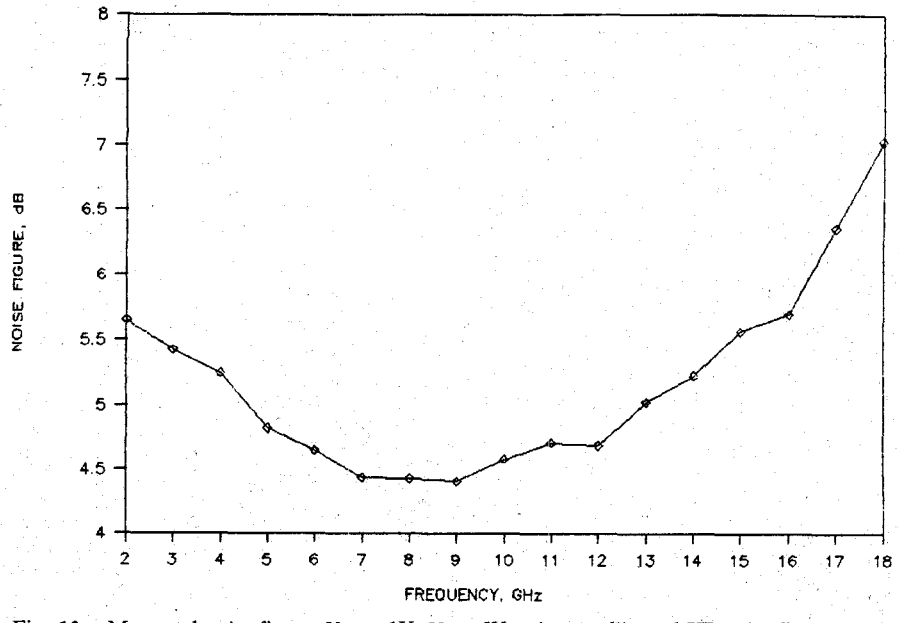

Fig. 13. Measured noise figure, $V_g = -1$V, $V_{ds} = 5$V, using a calibrated HP noise figure meter.

VI. Conclusions

Theoretical results using a normalized transmission matrix formulation for the distributed amplifier have been developed. This technique yields insight into amplifier operation because it displays the traveling-wave nature of the distributed amplifier. A gain expression for the commonly used *m*-derived topology has been derived as a special case of this technique. The expression is compared to a complex SuperCompact model of the amplifier and is seen to be optimistic by approximately 23 percent at midband. The error is due primarily to the unilateral assumption. Further refinements of the theory will include this effect.

The microstrip circuit design was found to be heavily dependent on available microstrip discontinuity and microstrip coupled line model accuracies. Several iterations were necessary to arrive at a physically consistent design.

The MMIC's are processed using ion implantation and e-beam lithography for the 0.5-μm gates. Good dc-to-RF yield has been observed.

Experimental results show excellent gain and return loss over 2–18.5 GHz with repeatable RF results.

Acknowledgment

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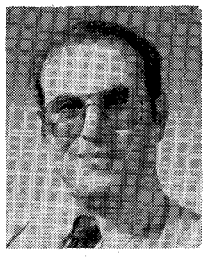
Tom McKay (M'80) was born in Milwaukee, WI, in 1960. He received the B.S.E.E. and M.S.E.E. degrees from the University of Wisconsin Madison, in 1982 and 1984. His master's work involved distributed amplifiers.

He joined Teledyne Monolithic Microwave shortly after it was formed in 1984 and began work on optimum distributed amplifier theory and design. He is also involved in FET and MMIC linear and nonlinear characterization and modeling.



John A. Eisenberg (M'68) was born in Jamaica, NY, in 1945. He received the B.S.E.E. and M.E.E. degrees from Cornell University in Ithaca, NY, in 1967 and 1968, respectively.

From 1968 to 1969, he was with Cayuga Associates in Ithaca, NY, where he developed a number of Gunn and IMPATT diode oscillators. In 1969, he joined Watkins Johnson Company, Palo Alto, CA. There his focus was the design of low-noise and medium-power microwave solid-state amplifiers. To aid in this work, he wrote one of the first general-purpose microwave circuit analysis and optimization programs. In 1972, he was made Head, Advanced Development Section, and directed a development program that led to the first commerically available 4–8-GHz and 8–12-GHz GaAs FET amplifiers.

In 1979, Mr. Eisenberg was a cofounder of Narda Microwave, Western Operations, now a subsidiary of Loral Corp., where he was Vice President and Technical Director. At Narda he directed the development of its product line of GaAs FET amplifiers, and the underlying gallium-arsenide and thin-film technologies. He was intimately involved with product development efforts, which resulted in the first commercially available 8–18-GHz, 6–18-GHz and 2–8-GHz bandwidth GaAs FET amplifier. These amplifiers formed the backbone of an extensive line of low-noise and medium-power GaAs FET amplifiers spanning the 2–18-GHz range.

In 1984, he formed John A. Eisenberg and Assoc., Los Altos, CA. and has practiced since that date as an independent consultant to various companies in the micrwave industry. His current efforts are largely directed at development and application of GaAs MMIC's.

Mr. Eisenberg is the author of numerous papers on topics related to solid-state microwave amplifiers.

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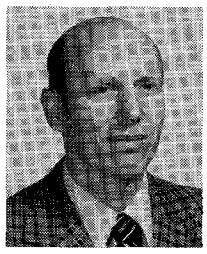

Ralph E. Williams (M'77–SM'83) received the Ph.D. degree in physics from the University of Maryland in 1976.

He joined the Central Research Laboratories of Texas Instruments that year to work on GaAs FET's. Dr. Williams helped develop the first GaAs MMIC and, more generally, was involved in all aspects of GaAs FET and MMIC research, emphasizing processing. He moved to the Defense System and Electronics Group (DSEG) of Texas Instruments in 1983 to help establish the DSEG GaAs Facility. He is now a Senior Member of the Technical Staff and engineering manager of the GaAs Facility.

Dr. Williams is the author of *Gallium Arsenide Processing Techniques.*